WHAT IS CLAIMED IS:

1. A capacitor comprising:

an insulating layer overlying a substrate;

a semiconductor layer overlying the insulator layer;

a bottom electrode formed in a portion of the semiconductor layer;

a capacitor dielectric overlying the bottom electrode, the capacitor dielectric comprising a high permittivity dielectric having a dielectric constant greater than about 5; and

a top electrode overlying the capacitor dielectric.

2. The capacitor of claim 1 wherein the capacitor is a decoupling capacitor.

3. The capacitor of claim 2 wherein the top electrode is connected to a power supply line and the bottom electrode is connected to a ground line.

4. The capacitor of claim 2 wherein the top electrode is connected to a first power supply line and the bottom electrode is connected to a second power supply line.

5. The capacitor of claim 1 wherein the bottom electrode or the top electrode is substantially flat.

6. The capacitor of claim 1 wherein the top electrode comprises poly-crystalline silicon.

7. The capacitor of claim 1 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

8. The capacitor of claim 1 wherein the top electrode comprises a metal nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, or combinations thereof.

9. The capacitor of claim 1 wherein the top electrode comprises a metal silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

10. The capacitor of claim 1 wherein the top electrode comprises a metal oxide selected from the group consisting of ruthenium oxide, indium tin oxide, or combinations thereof.

11. The capacitor of claim 1 wherein the high permittivity dielectric comprises hafnium oxide.

12. The capacitor of claim 1 wherein the high permittivity dielectric comprises a material is selected from the group consisting of aluminum oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, or combinations thereof.

13. The capacitor of claim 1 wherein the high permittivity dielectric has a relative permittivity of greater than about 10.

14. The capacitor of claim 1 wherein the high permittivity dielectric has a relative permittivity of greater than about 20.

15. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of less than about 100 angstroms.

16. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of less than about 20 angstroms.

17. The capacitor of claim 1 wherein the capacitor has a width of larger than about 5 microns.

18. The capacitor of claim 1 wherein the capacitor has a width of larger than about 10 microns.

19. The capacitor of claim 1 wherein the capacitor has a length of larger than about 1 micron.

20. The capacitor of claim 1 wherein the capacitor has a length of larger than about 5 microns.

21. The capacitor of claim 1 wherein the bottom electrode contact region is doped to the first conductivity type and wherein the bottom electrode is doped to a second conductivity type and coupled to a supply voltage that creates an inversion region of the first conductivity type.

22. The capacitor of claim 1 wherein the bottom electrode and the bottom electrode contact region are doped to the first conductivity type.

23. A decoupling capacitor comprising:

a semiconductor substrate comprising a silicon surface layer;

a substantially flat bottom electrode formed in a portion of the semiconductor surface layer;

a capacitor dielectric overlying the bottom electrode, the capacitor dielectric comprising a high permittivity dielectric with a relative permittivity greater than about 5;

a substantially flat top electrode overlying the capacitor dielectric; and

wherein the top electrode is electrically coupled to a first reference voltage line and the bottom electrode is electrically coupled to a second reference voltage line.

24. The capacitor of claim 23 wherein the top electrode is connected to a power supply line and the bottom electrode is connected to a ground line.

25. The capacitor of claim 23 wherein the top electrode is connected to a first power supply line and the bottom electrode is connected to a second power supply line.

26. The capacitor of claim 23 wherein the semiconductor substrate is a bulk silicon substrate.

27. The capacitor of claim 23 wherein the semiconductor substrate is a silicon-on-insulator substrate.

28. The capacitor of claim 23 wherein the top electrode comprises silicon.

29. The capacitor of claim 23 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

30. The capacitor of claim 23 wherein the top electrode comprises a metal nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, or combinations thereof.

31. The capacitor of claim 23 wherein the top electrode comprises a metal silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

32. The capacitor of claim 23 wherein the high permittivity dielectric comprises hafnium oxide.

33. The capacitor of claim 23 wherein the high permittivity dielectric comprises a material selected from the group consisting of hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

34. The capacitor of claim 23 wherein the high permittivity dielectric has a relative permittivity of greater than 10.

35. The capacitor of claim 23 wherein the high permittivity dielectric has a relative permittivity of greater than 20.

36. The capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less than about 100 angstroms.

37. The capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less than about 50 angstroms.

38. The capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less than about 10 angstroms.

39. The capacitor of claim 23 wherein the capacitor has a width of larger than about 5 microns.

40. The capacitor of claim 23 wherein the capacitor has a width of larger than about 10 microns.

41. The capacitor of claim 23 wherein the capacitor has a length of larger than about 1 micron.

42. The capacitor of claim 23 wherein the capacitor has a length of larger than about 5 microns.

43. The capacitor of claim 23 wherein the bottom electrode is doped to a first conductivity type, the capacitor further comprising adjacent doped regions doped to a second conductivity type.

44. The capacitor of claim 43 wherein the first conductivity type is n-type and the second conductivity type is p-type.

45. The capacitor of claim 43 wherein the first conductivity type is p-type and the second conductivity type is n-type.

46. The capacitor of claim 23 wherein the bottom electrode is doped to a first conductivity type, the capacitor further comprising adjacent doped regions with the first conductivity type.

47. The capacitor of claim 23 and further comprising spacers formed on sides of the top electrode.

48. The capacitor of claim 47 and further comprising an etch-stop layer overlying the top electrode and the spacers.

49. The capacitor of claim 48 wherein the etch-stop layer comprises silicon nitride.

50. The capacitor of claim 48 and further comprising an inter-layer dielectric overlying the etch-stop layer.

51. The capacitor of claim 50 wherein the inter-layer dielectric comprises silicon oxide.

52. The capacitor of claim 50 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.5.

53. The capacitor of claim 50 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.0.

54. The capacitor of claim 50 wherein the inter-layer dielectric is selected from the group consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), and SiOF.

55. The capacitor of claim 50 and further comprising a first contact plug in electrical contact with the bottom electrode and a second contact plug in electrical contact with the top electrode.

56. The capacitor of claim 23 further comprising a shallow trench isolation region adjacent to the bottom electrode.

57. The capacitor of claim 23 wherein semiconductor substrate comprises a semiconductor on insulator substrate including a plurality of islands, wherein the islands are isolated from one another by mesa isolation.

58. A method of forming a capacitor, the method comprising:

providing a silicon-on-insulator substrate including a silicon layer overlying an insulator layer;

forming a bottom electrode in the silicon layer;

forming a capacitor dielectric on bottom electrode, the capacitor dielectric comprising a high permittivity dielectric with a relative permittivity greater than about 5;

forming a top electrode on capacitor dielectric;

forming a bottom electrode contact region within the strained silicon layer adjacent the bottom electrode; and

electrically connecting the bottom electrode and the bottom electrode contact region.

59. The method of claim 58 wherein the capacitor is a decoupling capacitor.

60. The method of claim 58 wherein the step of forming the bottom electrode comprises:

forming an active region;

forming isolation regions surrounding the active region; and

doping the active region.

61. The method of claim 60 wherein the active region has a doping concentration of greater than about $10^{19}cm^{-3}$.

62. The method of claim 58 wherein forming the capacitor dielectric comprises a chemical vapor deposition step.

63. The method of claim 58 wherein forming the capacitor dielectric comprises a sputtering deposition step.

64. The method of claim 58 wherein the step of forming the capacitor dielectric comprises:
forming an interfacial oxide layer; and
forming a high permittivity dielectric layer.

65. The method of claim 58 and further comprising:
doping a portion of the silicon layer not covered by top electrode;
forming spacers on sides of the top electrode; and
doping a portion of the silicon layer not covered by the top electrode and spacers.

66. The method of claim 65 wherein the spacers comprise silicon nitride.

67. The method of claim 65 further comprising:
depositing an etch-stop layer over top electrode and spacers;
forming an inter-layer dielectric over etch-stop layer;
forming contact holes in inter-layer dielectric; and
filling the contact holes with a conductive material to form contact plugs.

68. The method of claim 67 wherein the etch-stop layer comprises silicon nitride.

69. The method of claim 67 wherein the inter-layer dielectric comprises silicon oxide.

70. The method of claim 67 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.5.

71. The method of claim 67 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.0.

72. The method of claim 67 wherein the inter-layer dielectric is selected from the group consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), and SiOF.

73. The method of claim 67 wherein the contact plugs comprise a first contact plug that electrically contacts the bottom electrode and a second contact plug that electrically contacts the top electrode.

74. The method of claim 73 wherein the top electrode is electrically coupled to a power supply line and the bottom electrode is electrically coupled to a ground line.

75. The method of claim 73 wherein the top electrode is electrically coupled to a first power supply line and the bottom electrode is electrically coupled to a second power supply line.

76. The method of claim 58 wherein the insulator layer comprise silicon oxide.

77. The method of claim 58 wherein the insulator layer has a thickness of less than about 1200 angstroms.

78. The method of claim 58 wherein the silicon layer has a thickness of less than about 1000 angstroms.

79. The method of claim 58 wherein the top electrode comprises silicon.

80. The method of claim 58 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

81. The method of claim 58 wherein the top electrode comprises a metallic nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, or combinations thereof.

82. The method of claim 58 wherein the top electrode comprises a metallic silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

83. The method of claim 58 wherein the high permittivity comprises hafnium oxide.

84. The method of claim 58 wherein the high permittivity dielectric is selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, or combinations thereof.

85. The method of claim 58 wherein the high permittivity dielectric has a relative permittivity of greater than about 10.

86. The method of claim 58 wherein the high permittivity dielectric has a relative permittivity of greater than about 20.

87. The method of claim 58 wherein the capacitor dielectric has a physical thickness of less than about 100 angstroms.

88. The method of claim 58 wherein the capacitor dielectric has a physical thickness of less than about 50 angstroms.

89. The method of claim 58 wherein the capacitor dielectric has a physical thickness of less than about 10 angstroms.

90. The method of claim 58 wherein the capacitor has a width of greater than about 5 microns.

91. The method of claim 58 wherein the capacitor has a width of greater than about 10 microns.

92. The method of claim 58 wherein the capacitor has a length of greater than about 1 micron.

93. The method of claim 58 wherein the capacitor has a length of greater than about 5 microns.